

1	INPUT/OUTPUT DATA PROCESSING	49	... Masking
2	.Input/Output expansion	50	... Vectored
3	.Input/Output addressing	51	..Accessing via a multiplexer
4	.Address data transfer	52	.Input/Output data buffering
5	.Input/Output command process	53	..Alternately filling or emptying buffers
6	.Operation scheduling	54	..Queue content modification
7	..Concurrently performing Input/Output operation and other operation unrelated to Input/Output	55	..Contents validation
8	.Peripheral configuration	56	..Buffer space allocation or deallocation
9	..Address assignment	57	..Fullness indication
10	..Configuration initialization	58	.Input/Output process timing
11	..Protocol selection	59	..Processing suspension
12	..As input or output	60	..Transfer rate regulation
13	..By detachable memory	61	..Synchronous data transfer
14	..Mode selection	62	.Peripheral adapting
15	.Peripheral monitoring	63	..Universal
16	..Characteristic discrimination	64	..Via common units and peripheral-specific units
17	..Availability monitoring	65	..Input/Output data modification
18	..Activity monitoring	66	..Width conversion
19	..Status updating	67	..Keystroke interpretation
20	.Concurrent Input/Output processing and data transfer	68	..Data compression and expansion
21	..Concurrent data transferring	69	..Analog-to-digital or digital-to-analog
22	.Direct Memory Accessing (DMA)	70	..Digital-to-digital
23	..Programmed control memory accessing	71	..Serial-to-parallel or parallel-to-serial
24	..By command chaining	72	..Application-specific peripheral adapting
25	..Timing	73	...For user input device
26	..Using addressing	74	...For data storage device
27	..Via separate bus	100	INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
28	..With access regulating	300	.Bus expansion or extension
29	.Flow controlling	301	..Card insertion
30	.Frame forming	302	..Hot insertion
31	.Transfer direction selection	303	..Docking station
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34	..Transferred data counting	105	.Protocol
35	..Burst data transfer	106	..Using transmitter and receiver
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37	..Access dedication	108	..Bus locking
38	..Path selection	109	..Bus polling
39	..Access request queuing	110	..Bus master/slave controlling
40	..Access prioritization	111	..Rotational prioritizing (i.e., round robin)
41	...Dynamic	112	..Bus request queuing
42	...Group	113	..Centralized bus arbitration
43	...Physical position	114	...Static bus prioritization
44	...Prioritized polling		
45	...Time-slot accessing		
46	..Input/Output polling		
47	..Polled interrupt		
48	..Input/Output interrupting		

115Physical position bus
prioritization
116 ...Dynamic bus prioritization
117 ...Time-slotted bus accessing
118 ...Delay reduction
119 ..Decentralized bus arbitration
120 ...Hierarchical or multilevel
accessing
121 ...Static bus prioritization
122Physical position bus
prioritization
123 ...Dynamic bus prioritization
124 ...Time-slotted bus accessing
125 ...Delay reduction
305 .Bus interface architecture
306 ..Bus bridge
307 ...Variable or multiple bus width
308 ...Direct memory access (e.g.,
DMA)
309 ...Arbitration
310 ...Buffer or que control
311 ...Intelligent bridge
312 ...Multiple bridges
313 ...Peripheral bus coupling (e.g.,
PCI, USB, ISA, and etc.)
314 ...Common protocol (e.g., PCI to
PCI)
315 ...Different protocol (e.g., PCI
to ISA)
316 ..Path selecting switch
317 ...Crossbar
200 **ACCESS LOCKING**
220 **ACCESS POLLING**
240 **ACCESS ARBITRATING**
241 .Centralized arbitrating
242 .Decentralized arbitrating
243 .Hierarchical or multilevel
arbitrating
244 .Access prioritizing
260 **INTERRUPT PROCESSING**
261 .Multimode interrupt processing
262 .Interrupt inhibiting or masking
263 .Interrupt queuing
264 .Interrupt prioritizing
265 ..Variable
266 .Programmable interrupt
processing
267 .Processor status
268 .Source or destination identifier
269 .Handling vector

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